# 60-GHz GaAs MMIC LOW-NOISE AMPLIFIERS*

H-L. A. Hung, T. T. Lee, F. R. Phelleps, J. F. Singer,
J. F. Bass, T. F. Noble, and H. C. Huang
COMSAT Laboratories, Clarksburg, Maryland 20871-9475

and

P. Rainville
Rome Air Development Center, Hanscom AFB, Massachusetts 01731-5000

## ABSTRACT

GaAs monolithic MESFET low-noise amplifiers (LNAs) have been developed at V-band. A single-stage MMIC has achieved a 6.4-dB noise figure and 3.5-dB gain at 59 GHz. A cascaded six-stage amplifier exhibited 9.5-dB minimum noise figure and 26-dB gain from 56 to 60 GHz. These data may represent the first reported results of MMIC LNAs in the 60-GHz band with DC-blocking and bias networks.

## INTRODUCTION

Millimeter-wave field-effect transistor (FET) low-noise amplifiers (LNAs) are currently being developed for potential application in intersatellite link and electronic warfare systems. Discrete modulation-doped FET (MODFET) devices have shown excellent noise performance at V-band [1]. A 30-GHz monolithic metal semiconductor FET (MESFET) LNA with 7-dB noise figure and 14-dB gain has also been presented [2]. Recently, a single-stage monolithic MODFET LNA was reported at 44 GHz [3], while Kim et al. [4] have reported the gain result of a V-band power monolithic microwave integrated circuit (MMIC) with a 100-μm gate-width MESFET. Because no input and output DC-blocking elements were included in these designs, and because bias networks were also omitted in some cases, direct cascading of the MMICs to achieve usable gain is not possible.

This paper presents new data regarding the use of MESFET LNAs for the 60-GHz band. A device/circuit CAD program developed at COMSAT Laboratories permitted a parametric study of circuit performance, with variation of the device structure and material parameters prior to MMIC fabrication. Single- and dual-stage LNA modules with DC-blocking capacitors and bias networks were developed from the first design iteration. A cascaded multistage monolithic amplifier having stable operation was also achieved. The RF results obtained demonstrated the application of MESFETs in single- and multi-stage MESFET MMIC LNAs, with good noise performance and usable gain at V-band.

## DEVICE AND CIRCUIT DESIGN

The MESFET used in this study (Figure 1) had a total gate-width of 60 μm and a dual-fed gate with a nominal length of 0.3 μm. A structure was first established by evaluating the performance of an equivalent circuit model of the MESFET, generated by a device-modeling computer program based on device physics, geometry, and material parameters. High doping density for the active region and an optimized gate-length to channel-height ratio were used.

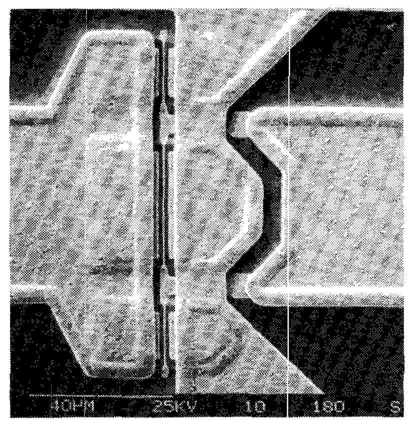


Figure 1. Scanning Electron Micrograph of a MESFET From the V-Band MMIC

The input circuit of the single-stage amplifier was designed to provide a source impedance to the MESFET, resulting in low noise performance. The output circuit, which included RF-shorted and open shunt elements, was then optimized for output return loss and gain flatness across the desired frequency band. A transmission line model of the input and output DC-blocking capacitors was used to account for their distributive characteristics. Input and output biases were provided by the shunt RF-shorted elements, which were grounded through metal-insulator-metal (MIM) capacitors and via-holes The monolithic MIM capacitor model and the

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parasitic inductance associated with via-holes were included in the circuit analysis. In the two-stage design, the interstage matching network was used to optimize the bandwidth and gain flatness of the amplifier.

At millimeter-wave frequencies, some uncertainty exists regarding the accuracy of commercially available circuit analysis programs, as well as the prediction of associated device and circuit parasitics. A design approach was established that allowed slight adjustment of the matching circuits without additional mask fabrication, after a preliminary circuit evaluation. Tuning islands were incorporated into a circuit layout which could then be connected via the direct e-beam writing technique. By carefully planning the circuit layout during mask design, the same scheme allowed the connection of different stages of MMICs to obtain multistage amplifiers on a single chip. This approach enabled the designed performance to be achieved without any mask iterations.

## MMIC FABRICATION

COMSAT's baseline mesa MMIC process (similar to that previously reported [5], with sequence variation) was used to fabricate the monolithic amplifiers. Photolithography techniques, and e-beam direct-write for the gate structures, were employed. Layers of $n^+$/n/buffer structure were grown on Bridgman semi-insulating material by vapor phase epitaxy. A rapid-thermal annealed Au/Ge/Ni/Ag/Au alloy and an evaporated Ti/Pt/Au metalization were used for the ohmic contacts and gates, respectively. The $Si_3N_4$ dielectric for the MIM capacitor and device passivation were deposited by plasma-enhanced chemical vapor deposition (PECVD). The air-bridge structures and transmission lines were fabricated using two mask levels: plating-via and plating. Through-substrate via-holes were obtained by infrared and spray etch techniques to provide low-inductance grounding for the MESFET sources and the shorted shunt elements. The chip sizes for the single- and dual-stage MMICs are 1.6 x 0.75 x 0.08 mm and 2 x 0.75 x 0.08 mm, respectively. Figure 2 shows a sample single-stage LNA.

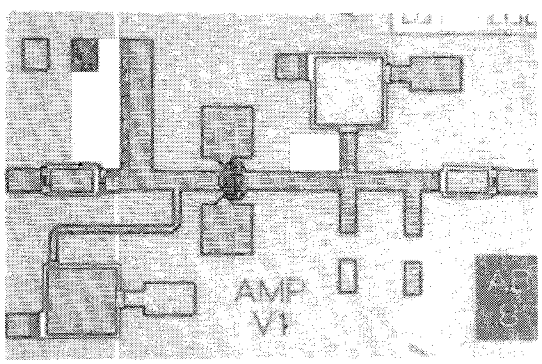


Figure 2. Single-Stage MMIC LNA

## MEASURED PERFORMANCE

To accurately measure the performance of the MMICs, V-band waveguide-to-microstrip transitions were developed using antipodal finline structures on 0.127-mm-thick fused-silica substrates. The measured insertion loss and return loss of one waveguide-to-microstrip transition were 0.5 to 0.7 dB, and better than 18 dB, respectively, from 50- to 60-GHz.

The MMICs were mounted on the metal test fixture, which included bias feedthroughs and a short (2.5-mm) 50-Ω line at the input and output of the monolithic circuits for ease of assembly and disassembly. This evaluation approach allowed modules to be cascaded in a multistage amplifier configuration. The RF loss of the 50-Ω transmission line was included in the measured results. Figure 3 shows an assembled two-stage MMIC LNA with waveguide-to-microstrip transitions. A Hewlett-Packard 40- to 60-GHz measurement set-up was used to obtain the frequency response. This was supplemented by the Hughes millimeter-wave systems to measure gain response at higher frequencies and power performance. The noise-figure was measured using the hot-and-cold load technique.

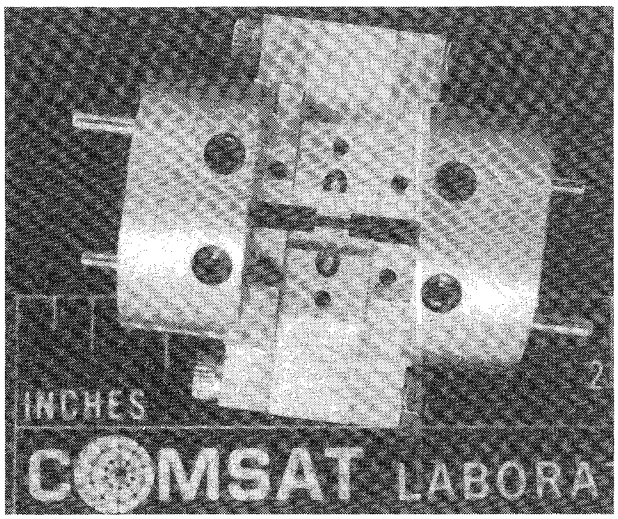


Figure 3. Sample Assembly of the V-Band Two-Stage MMIC With Waveguide-to-Microstrip Transitions

Figure 4 shows the measured performance of a single-stage LNA. A small signal gain of 3.2 to 5.0 dB was obtained from 52.5 to 60 GHz. A noise figure of 6.4 dB and an associated gain of 3.5 dB were achieved at 59 GHz. The nominal bias parameters of the devices are a drain voltage of 3 V and a drain current of 9 to 12 mA.

Figure 5 depicts the results of the two-stage MMIC amplifier. Linear gain of better than 9 dB and a minimum noise figure of 8.9 dB were obtained in the frequency range of 55 to 60 GHz. The modules could provide more than 10-dB gain at a higher bias drain current, and an output power of better than 12 dBm. Figure 6 shows the output vs input power of a two-stage MMIC. A power density of 0.27 W/mm has been achieved at 1-dB gain compression.

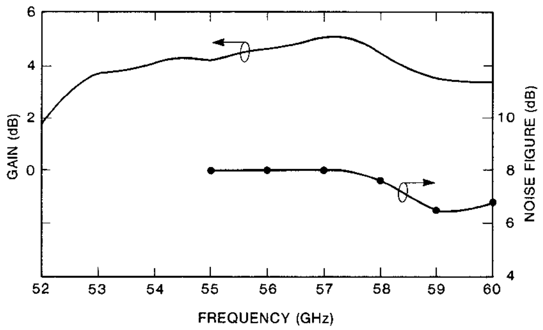


Figure 4. Noise Figure and Gain vs Frequency of a Single-Stage MMIC LNA

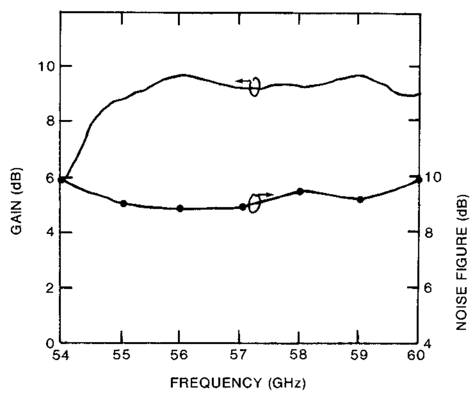


Figure 5. Performance of a Two-Stage MMIC LNA

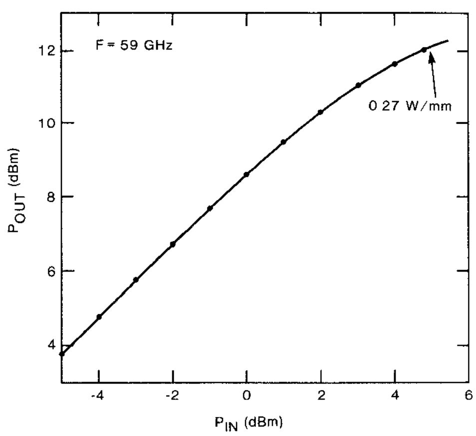


Figure 6. $P_{out}$ vs $P_{in}$ of a Two-Stage MMIC Amplifier

To achieve usable gain for system applications, MMIC modules were cascaded. A six-stage amplifier exhibited a noise figure of 9.5 to 9.9 dB and an associated linear gain of 26 dB across the 56- to 60-GHz band, as illustrated in Figure 7. Stable operation was obtained with this amplifier.

Recent measurements have indicated that the bandwidth of these amplifiers can be extended to 62 GHz. Furthermore, the performance of a two-stage MMIC from wafer runs with higher carrier doping concentrations ($5 \times 10^{17}$ $cm^{-3}$) showed improvement in both the minimum noise figure (by 1 dB) and associated linear gain (by 2 dB).

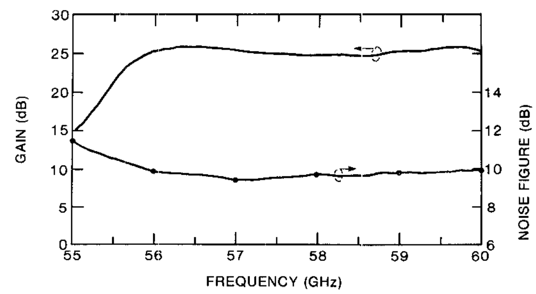


Figure 7. Noise and Associated Gain Performance of the Six-Stage MMIC LNA

## CONCLUSIONS

Monolithic single- and dual-stage LNAs using MESFETs were designed and fabricated. Excellent RF performance has been demonstrated over a wide frequency band to beyond 60 GHz. These results may represent the first low-noise data reported for MESFET single and multistage monolithic amplifiers with built-in DC-blocking and bias networks at V-band. The work presented in this paper, and recent power results [6], demonstrate the potential for using MESFET MMIC technology for future millimeter-wave systems such as satellite communications and electronic warfare applications.

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